James G. Ryan, Ph.D.

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North Carolina A&T and the University of North Carolina-Greensboro
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Current Position – (7/08 to Present)

Founding Dean of the Joint School of Nanoscience and Nanoengineering of North Carolina A&T State University and the University of North Carolina at Greensboro. Responsibilities include academic and administrative leadership of JSNN as well as the development of strategic partnerships with industry and government organizations. Research interests include thin film deposition, interconnect technology, semiconductor manufacturing technology and radiation hardened nanoelectronics.

Education

Degree	Field	University	Date Conferred
PhD	Chemistry	Rensselaer Polytechnic Institute	1988
MS	Biomedical Eng.	Rensselaer Polytechnic Institute	1980
MS	Chemistry	Rensselaer Polytechnic Institute	1978
BS	Chemistry	Rensselaer Polytechnic Institute	1977

CNSE Career Highlights (2/05 – 6/08)

- 10/05–6/08 Director & Principal Investigator, Radiation Hardened Nanoelectronics Focus Center (NRL grant)
- 6/05 – 6/08 Director & Co-PI, Center for Semiconductor Research (CNSE – IBM R&D Agreement)
- 2/05 – 6/08 Director, Program Executive, International SEMATECH North (CNSE – SEMATECH R&D Agmt)
- 2/05 – 6/08 Vice President of Technology, Albany Nanotech
- 2/05 - 6/08 Associate Vice President of Technology, CNSE
- 10/07-6/08 Chair, CNSE Research Committee
- Lead negotiator & PI / Co-PI for ~$2.0 Billion in contracts with IBM, SEMATECH, ASML, AMAT, TEL and Ebara

Board Positions

- 10/07 – Present Scientific advisory board member, NaMLaB (Qimonda & TU of Dresden's Joint Venture)
- 10/09 – Present Member, Center for Innovation in Nanobiotechnology (COIN) Board of Directors
- 11/07 – 6/08 Member, SEMATECH Board of Directors

IBM Career Highlights (1979 – 2005)

- IBM's director and site executive for its strategic interaction with CNSE until 2/05
- Led interconnection technology genesis groups for IBM's 0.35μm, 0.25μm, 0.13 μm & 0.10 μm nodes.
- First implementation of Cu wiring in development line, led team that developed protocols for controlling cross contamination risks still in use today (received Outstanding Technical Achievement Award)
- Implemented damascene wiring technology in 0.35μm increasing yield and productivity (received Outstanding Technical Achievement Award)
- Invented Fluorinated Glass deposition technique that became the standard of the microelectronics industry (received Corporate Patent Portfolio Award)
- Invented Collimated Liner Process for contacts and wiring that was widely used in microelectronics (received Microelectronics Division Patent Portfolio Award)
- IBM Master Inventor (47 U.S. Patents), Managed IBM's "benchmark" group for innovation, drove a fivefold increase in invention disclosure output
- Authority in interconnect technology & materials science (Over 100 papers, presentations, etc.)

Employment History

2005-2008 Associate Vice President of Technology and Professor of Nanoscience in the College of Nanoscale Science and Engineering (CNSE) of the University at Albany.
- Responsibilities included development of strategic relationships and managing operations of the cleanrooms and consortia at CNSE.
- Research interests include thin film deposition, interconnect technology, semiconductor manufacturing technology and radiation hard nanoelectronics.

2002-2005 Distinguished Engineer and Director of IBM @ Albany NanoTech, Albany, NY
- IBM’s site executive
- Responsible for the strategy and operations of IBM's R & D programs at CNSE.

1998-2002 Distinguished Engineer and Project Manager, Advanced Interconnect Technology, IBM Yorktown Heights, NY
- Supervised ~60 (5 managers, 55 research staff, engineers & technicians)
- Responsibilities included: Interconnect technology strategy, roadmap development, execution of advanced materials science research and technology genesis activity in interconnect technology
- Management responsibility for budget, personnel development and administration.

1994-1998 Senior Technical Staff Member and Project Manager, ASTC BEOL Engineering, IBM East Fishkill, NY
- Supervised ~60 (4 managers, 56 engineers & technicians).
- Responsibilities included: Interconnect technology development (including PVD, CVD, CMP, spin-on insulators, annealing, wet cleaning, BEOL integration and Cu BEOL), manufacturing support, equipment development/improvement and maintenance for 0.18μm through 0.5μm product generations in IBM's Advanced Semiconductor Technology Center.
- Management responsibility for budget, personnel development and administration.

1992-1994 Senior Engineering Manager, Thin Film and CMP Development, IBM-Siemens-Toshiba 256Mb DRAM Alliance, IBM East Fishkill, NY
- Supervised 23 people (11 IBM, 8 Toshiba, 4 Siemens; 8 PhD's, 9 MS, 3 BS, 3 AS)
- Responsibilities included: 0.25μm interconnect technology development, including advanced unit process and equipment development for PVD, CVD, CMP, Passivation, Redundancy technology, BEOL Integration and Reliability
- Administration of capital budget including vendor negotiation, Personnel development/administration

1990 - 1992 Manager Interconnection Technology, IBM Essex Junction, VT
- Supervised 9 people (6 PhD's, 2 BS, 1 AS)
- Responsible for 0.35μm technology transfer and 0.25μm technology genesis for contacts and wiring levels including advanced unit process development for PVD, CVD, CMP, Redundancy technology, BEOL Integration and Reliability

1988 - 1990 Advisory Engineer - Interconnection Technology, IBM Essex Junction, VT
- Lead Engineer responsible for 0.35μm wiring technology genesis/integration
- Projects included: Interconnect integration, Development of collimated sputtering technology, Implementation of damascene wiring technology, Silicide film development

1981-1988 Associate/Senior Associate/Staff Engineer – Interconnect Development, IBM, Essex Junction, VT
- Responsible for PVD and Metallization process for 1.0μm logic technology
- Projects included: Al RIE technology integration, Redundancy integration (laser deleted fuses), Research on stress induced voiding in Al alloys, Investigation of Ti-Al film interdiffusion and reactions Synthesis and characterization of refractory thin films including high dielectric constant oxides, metal borides as diffusion sources/barriers, metal nitrides and silicides, PVD (evaporation and sputtering) development including Al203 and Ti/TiN Liners for CVD W metallization, Development of RIE/PVD cluster tool, Invented Al bump final metallization for IBM's tape automated bonding technology

1979 - 1981 Associate Engineer - BEOL Etch Technology Development 64K DRAM, IBM East Fishkill, NY
- Responsible for nitride and polyimide plasma etch process development

Continuing Education

· Applied Materials Technology - Materials Processing for Process Sensitive Manufacturing - MIT (1985)
· Communication Excellence (1993)
· Working with the Japanese (1993)
· Numerous management/leadership/quality short courses

Technical Vitality Summary

- 47 Issued U.S. Patents, 17 IBM Invention Achievement Awards
- Over 100 papers, presentations and technical disclosures
- IBM Essex Junction representative to the SEMATECH Thin Film FTAB 1990-1991
- Member Industry Advisory Board for Clarkson University's Center for Advanced Materials Processing ('96 – '00)
- Member Industry Advisory Board for the University of Michigan's Materials Science Department (1998)
- Adjunct Professor of Physics at the University at Albany – SUNY ('94 – '98)
- Chair Industry Advisory Board for the Center for Advanced Technology at the University at Albany - SUNY (1996-1997)
- Chair for Advanced Metallization Session at ICMC-TF 1993-1998
- Co-Chair for Clarkson University's Annual CMP Meeting (1997 & 1998)
- Taught IBM internal graduate level course "Integrated Circuit Fabrication" (5 semesters)
- Taught graduate level Physics course "Integrated Circuit Manufacturing Technology" at the University at Albany - SUNY
- Taught "Multilevel Interconnect Technology" at SPIE's 1997 Symposium & Education Program on Microelectronic Mfg
- Lecturer for "Integrated Circuit Manufacturing Technology" for The Center for Professional Advancement
- Judge for *Small Times* "2007 Best of Small Tech" Awards
- 2008 CMP-MIC Executive Program Committee

Awards

- First Invention Achievement Award 9/83, Seventeenth Invention Achievement Award 12/04
- IBM's Top Inventor (1992)
- IBM Master Inventor
- Best IBM Burlington Paper Award (1987) for R.M. Geffken, J.G. Ryan and G.J. Slusser, "Contact Metallurgy Development for VLSI Logic", IBM Journal of Research and Development, 31, 608 (1987)
- Outstanding Paper, 1984 International Society for Testing and Failure Analysis Symposium for R. Douse, L. Hahn, M. Luciano, and J.G. Ryan, "Analytical Techniques and Procedures to Successfully Analyze Metal Step Coverage on Semiconductors", Proceedings of the International Symposium for Testing and Failure Analysis, 124 (1984)
- IBM Patent Portfolio Award for U. S. Patent 5,401,675, P.-I. Lee, T. Licata, T. McDevitt, P. Parries, S. Pennington, J. G. Ryan & D. Strippe, "Method Depositing Conductors in High Aspect Ratio Aperatures Using a Collimator," (1/98)
- Outstanding Technical Achievement Award for "Damascene Wiring Technology Innovation and Implementation," (6/98)
- Outstanding Technical Achievement Award for "Contributions to Copper Technology Development," (6/99).
- Corporate Headquarters Excellence Award for Recruiting (12/99)
- Corporate Patent Portfolio Award for U. S. Patent 5,563,105, D. Dobuzinsky, S. Nguyen, J. G. Ryan, M. Shapiro & T. Matsuda, "PECVD Method of Depositing Fluorine Doped Oxide Using a Fluorine Precursor Containing a Glass Forming Element." (5/04)
- The SRC 1999 Mahboob Khan Mentor Award for Contributions to Student Mentoring
- Named as one of "The Triad's Most Influential People (2009)" by The Business Journal.

Professional Societies

American Chemical Society
American Vacuum Society
Electrochemical Society

Citizenship

U.S. Citizen

Patents and Patent Applications

- J. E. Cronin, J. Hiltebeitel, C. W. Kaanta and J. G. Ryan, "Integrated Circuit Chip Wiring Structure with Crossover Capability and Method of Manufacturing the Same," U. S. Patent 6,576,848, Issued 6/10/03.
- B. El-Kareh and J. G. Ryan, "Flexible Interconnections with Dual-Metal Dual-Stud Structure," U.S. Patent 6,426,544, Issued 7/30/02.
- J. G. Ryan, A. Mitwalsky and K. Okumura, "Planarized Final Passivation for Semiconductor Devices," U. S. Patent 6,376,911, Issued 4/23/02.
- H. Jones and J. G. Ryan, "Technique for Extending the Limits of Photolithography," U. S. Patent 6,337,516, Issued 1/8/02.
- E. Levine, M. Lofaro, and J. G. Ryan, "Manufacturing Methods and Uses for Micro Pipe Systems," U. S. Patent 6,228,744, Issued 5/8/01.
- A.Chakravarti, S. Chakravarti, and J. G. Ryan, "A Process for Forming a High Density Semiconductor Device U. S. Patent 6,204,112, Issued 3/20/01.
- N. Greco, E. N. Levine, M. F. Lofaro, and J. G. Ryan, "Manipulation of Micromechanical Objects," U.S. Patent 6,199,269, Issued 3/13/01.
- B. El-Kareh, A. El-Kareh and J. G. Ryan, "Capacitor Charging Sensor," U.S. Patent 6,144,037, Issued 11/7/00.
- H. Jones and J. G. Ryan, "Technique for Extending the Limits of Photolithography," U. S. Patent 6,140,217, Issued 10/31/00.
- N. A. Greco, E. N. Levine, M. F. Lofaro, and J. G. Ryan, "Casting of Complex Micromechanical Objects," U. S. Patent 6,098,788, Issued 8/8/00.
- E. Levine, M. Lofaro, and J. G. Ryan, "Semiconductor Structures Containing a Micro Pipe System," U. S. Patent 6,031,286, Issued 2/29/00.
- B. El-Kareh and J. G. Ryan, "Flexible Interconnections with Dual-Metal Dual-Stud Structure," U. S. Patent 5,972,788, Issued 10/28/99.
- J. P. Gambino, M. Peschke, J. G. Ryan, "Borderless Contact Etch Process with Sidewall Spacer and High Selective Isotropic Etch Process, U. S. Patent 5,960,318, Issued 9/28/99.
- B. El-Kareh, J. A. Mandelman, and J. G. Ryan, "Method for Electrostatic Discharge Protection Through Electric Field Emission," U. S. Patent 5,933,718, Issued 8/3/99.
- A.Chakravarti, S. Chakravarti, and J. G. Ryan, "A Process for Forming a High Density Semiconductor Device," U. S. Patent 5,909,044, Issued 6/1/99.
- J. Hsieh, D. M. Kenney, T. J. Licata and J. G. Ryan, "Method for Selective Material Deposition on One Side of Raised or Recessed Features," U. S. Patent 5,885,425, Issued 3/23/99.
- A. Mitwalsky, J. G. Ryan and T. Wassick, "Ablation Patterning of Multi-layered Structures," U. S. Patent 5,843363, Issued 12/1/98 (divisional application).
- A. Mitwalsky and J. G. Ryan, "Crack Stop Formation for High Productivity Processes," U.S. Patent 5,776,826, Issued 7/7/98.
- A. Mitwalsky, J. G. Ryan and T. Wassick, "Ablation Patterning of Multi-layered Structures," U.S. Patent 5,766,497,

Issued 6/16/98.

- B. El-Kareh, H. Tanimoto and J. G. Ryan, "Latch-Up Reduction by Schottky-Barrier Clamping in an ESD Structure," U.S. Patent 5,763,918, Issued 6/9/98.
- R.V. Joshi, K. Kimmel, T. J. Licata, and J. G. Ryan, "Tungsten Absorber X-ray Mask," U.S. Patent 5,757,879, Issued 6/9/98.
- V. McGahay, J.G. Ryan, M. Shapiro, and C. Waskiewicz, "Method and Apparatus for Determining Chamber Cleaning End Point," U. S. Patent 5,712,702, Issued 1/27/98.
- R. Kontra, T. J. Licata, J. G. Ryan, and T. D. Sullivan, "Process for Depositing a Conductive Thin Film Upon an Integrated Circuit Substrate," U. S. Patent 5,711,858, Issued 1/27/98.
- K. Okumura, J. G. Ryan, G. B. Stephenson and H. G. Timme, "In-Situ Temperature Measurement Using X-ray Diffraction," U. S. Patent 5,636,258, Issued 6/3/97.
- W.J. Cote, K. Okumura, J.G. Ryan, and H. Yano, "Apparatus for Processing Semiconductor Wafers," U. S. Patent 5,593,537, Issued 1/14/97.
- A. Mitwalsky and J. G. Ryan, "Improved Fuse Link Structures through the Addition of Dummy Structures," U.S. Patent 5,589,706, Issued 12/31/96.
- D.M. Dobuzinsky, S.V. Nguyen, J.G. Ryan, M. Shapiro, and T. Matsuda, "Method of Depositing Fluorine Doped Oxide," U.S. Patent 5,563,105, Issued 10/8/96.
- W. J. Cote, K. Okumura, J. G. Ryan, and H. Yano, "Apparatus for Processing Semiconductor Wafers," U.S. Patent 5,534,106, Issued 7/9/96.
- J.G. Ryan, D. Strippe and B. Vollmer, "Method of Depositing Conductors in High Aspect Ratio Aperatures Under High Temperature Conditions," U. S. Patent 5,529,670, Issued 6/25/96.
- P-I. Lee, T. Licata, T. McDevitt, P. Parries, S. Pennington, J. G. Ryan and D. Strippe, "Method of Depositing Conductors in High Aspect Ratio Aperatures," U. S. Patent 5,401,675, Issued 3/28/95.
- P. J. Geiss, H. Ho, T. J. Licata, and J. G. Ryan, "Epitaxial Cobalt Silicide Formed Using a Thin Metal Underlayer," U. S. Patent 5,356,837, Issued 10/18/94.
- J. E. Cronin, P. A. Farrar, Sr., C. W. Kaanta, J. G. Ryan, and A. J. Watts, "Gray Level Mask," U. S. Patent 5,334,475, Issued 8/2/94.
- J. E. Cronin, R. A. Previti-Kelly, J. G. Ryan, T. D. Sullivan, "Cooling Microfan Arrangements and Process," U.S. Patent 5,326,430, Issued 7/5/94.
- J. E. Cronin, R. A. Previti-Kelly, J. G. Ryan, T. D. Sullivan, "Cooling Microfan Arrangements and Process," U. S. Patent 5,296,775, Issued 3/22/94.
- B.N. Agarwala, A. M. Ahsan, A. Bross, M.F. Chadurjian, M.G. Koopman, L. Lee, K.J. Puttlitz, S. K. Ray, J. G. Ryan, J. G. Schaefer, K.K. Srivastava, P. A. Totta, E.G. Walton, and A. E. Wirsing, "An Elongated Solder Interconnection and a Method for Making Same," U. S. Patent 5,521,806, Issued 10/12/93.
- J. E. Cronin, C. W. Kaanta, P.P. Lee, R. Previti-Kelly, J. G. Ryan, and J. Yoon, "Process for Forming Multi-Level Coplanar Conductor/Insulator Films Employing Photosensitive Polyimide Polymer Compositions," U. S. Patent 5,229,257, Issued 7/20/93.
- J. E. Cronin, P. A. Farrar, Sr., C. W. Kaanta, J. G. Ryan, and A. J. Watts, "Gray Level Mask," U.S. Patent 5,213,916, Issued 5/25/93.

- M. J. Brady, S. K. Kang, P. A. Moskowitz, J. G. Ryan, T. C. Reiley, E. G. Walton, H. R. Bickford, and M. J. Palmer, "Aluminum Bump, Reworkable Bump, and Titanium Nitride Structure for TAB Bonding," U. S. Patent 5,134,460, Issued 7/28/92.

- B. N. Agarwala, A. M. Ahsan, A. Bross, M. F. Chadurjian, N. G. Koopman, L. Lee, K. J. Puttlitz, S. K. Ray, J. G. Ryan, J. G. Schaefer, K. K. Srivastava, P. A. Totta, E. G. Walton, and A. E. Wirsing, "Solder Mass Having Conductive Encapsulating Arrangement," U. S. Patent 5,130,779 Issued 7/14/92.

- W. Guthrie, C. Kaanta, J. Cronin, A. Watts, P. Farrar, R. Geffken, R. Previti-Kelly, J.G. Ryan, and R. Uttecht, "Plural Level Chip Masking," U. S. Patent 5,126,006, Issued 6/30/92.

- T. Faure, K. Kimmel, J. G. Ryan, T. D. Sullivan, "Process for X-ray Mask Warpage Reduction," U.S. Patent 5,124,561, Issued 6/23/92.

- J. E. Cronin, C. W. Kaanta, R. Previti-Kelly, and J. G. Ryan, "Process for Forming Multi-Level Coplanar Conductor/Insulator Films Employing Photosensitive Polyimide Polymer Compositions," U.S. Patent 5,091,289, Issued 2/25/92.

- S. B. Brodsky, R. V. Joshi, J. S. Lechaton, J. G. Ryan, and D. J. Schepis, "Method of Making Semiconductor Device Contact Including Transition Metal-Compound Dopant Source," U.S. Patent 5,086,016, Issued 2/4/92.

- D.A. Gardner, J. G. Ryan, J. G. Schaefer, and E. G. Walton, "Chromium-Titanium Alloy," U. S. Patent 4,840,302, Issued 6/20/89.

- M. H. Ishaq, S. Roberts, and J. G. Ryan, "Method for Making Diffusions into a Substrate and Electrical Connections Thereto Using Rare Earth Boride Materials," U.S. Patent 4,490,193, Issued 12/25/84.

- D.P. Bouldin, D.P. Hallock, S. Roberts, and J. G. Ryan, "Method for Making Diffusions into a Substrate and Electrical Connections Thereto using Silicon Containing Rare Earth Hexaboride Materials, U.S. Patent 4,481,046, Issued 11/6/84.

- S. Roberts and J. G. Ryan, "Process for Making High Dielectric Constant Nitride Based Materials and Devices Using the Same," U. S. Patent 4,464,701, Issued 8/7/84.

- M. Hakey, S. Holmes, D. Horak and J. G. Ryan, “Chemical and Particulate Filters Containing Chemically Modified Carbon Nanotube Structures,” Patent Pending, Filed 11/04.

- J. Fitzsimmons, V. McGahay, B. Chen and J. G. Ryan, "Plasma Processing Material Reclamation and Reuse," Patent Pending, Filed 6/03.

- K. Petrarca, M. Lagus, M. Krishnan and J. G. Ryan, "Method for Fabricating a Scanning Probe Microscope Probe," Patent Pending, Filed 1/02.

- J. Rubino, C. Jahnes, E. Liniger, J. G. Ryan, C. Sambucetti, F. Cardone, S. Purushothaman, J. Fitzsimmons and S. Gates, "Method for Forming Dual-Layer Low Dielectric Barrier for Interconnects and Device Formed," Patent Pending, Filed 2/22/00.

- H. Jones and J. G. Ryan, "Method and Apparatus for Forming Vertical Insulators," Patent Pending, Filed 12/17/99.

- H. Jones and J. G. Ryan, "Method and Apparatus for Forming Vertical Insulators with Central Pillars," Patent Pending, Filed 12/17/99.

- J. E. Cronin, C. W. Kaanta, R. Previti-Kelly, and J. G. Ryan, "Process for Forming Multi-level Coplanar Conductor/Insulator Films Employing Photosensitive Polyimide Polymer Compositions," Patent Application Filed 12/9/91 (divisional application).

- R. Kontra, T. J. Licata, J. G. Ryan, and T. D. Sullivan, "Integrated Circuit Element Comprising an Aluminum Alloy

Produced by a Directionally Controlled Deposition Process," Patent Application Filed 6/9/94, Abandoned 7/8/96 (divisional application).

- J. E. Cronin, C. W. Kaanta, P.P. Lee, R. Previti-Kelly, J. G. Ryan, and J. Yoon, "Process for Forming Multi-level Coplanar Conductor/Insulator Films Employing Photosensitive Polyimide Polymer Compositions," Patent Application, Filed 4/13/93, Abandoned 4/3/95 (divisional application).

- S. B. Brodsky, R. V. Joshi, J. S. Lechaton, J. G. Ryan, and D. J. Schepis, "Transition Metal-Compound Dopant Source and Semiconductor Device Contact," Patent Application Filed 10/28/91, Abandoned 1/8/93 (divisional application).

Publications

- A. E. Kaloyeros, M. R. Stan, R. Geer, E. T. Eisenbraun, J. Hartley, J. Raynolds, A. Gadre and J. G. Ryan, “Conformational Molecular Switches for Post-CMOS Nanoelectronics,” IEEE Tranactions on Circuits and Systems – I: Regular Papers, Special Issue on Nanoelectronic Circuits and Nanoarchitectures, 54 (11), pp. 2345 - 2352, 2007.

- A. E. Kaloyeros, J. Castracane, K. Dunn, E. Eisenbraun, A. Gadre, V. LaBella, T. Stoner, A. Topol, B. Xu and J. G. Ryan, “Summary and Foresight,” book chapter submitted for publication in Advanced Nanoscale ULSI Interconnects – Fundamentals and Practice, Y. Shacham, editor.

- S. Nitta, S. Purushothaman, P. Andricacos, D. Edelstein, J. Lloyd, R. Rosenberg, and J. G. Ryan, "Copper BEOL Interconnects for Silicon CMOS Logic Technology," book chapter in Interconnect Technology and Design for Gigascale Integration, edited by J. Davis and J. Meindl, Kluwer Academic Publishers, Boston, 2003.

- A. Krishnamoorthy, K. Chandra. S. P. Muruarka, G. Ramanath and J. G. Ryan, "Self-assembled near-zero-thickness molecular layers as diffusion barriers for Cu metallization," Applied Physics Letters, 78 (17), 2467 (2001).

- J. C. Hedrick, E. Barth, G. A. Biery, S. Cohen, T. Dalton, Davis, D. Edelstein, S. Gates, K. W.Lee, V. McGahay, C. Narayan, C. Davis, D. Edelstein, S. Gates, K. W.Lee, V. McGahay, C. Narayan, S. Nitta, H. Nye, S. Purushothaman, D. Restaino, E. Simonyi, C. Tyberg, R. Goldblatt and J. Ryan, "High Performance SiLK/Copper Interconnects," (invited) Proceedings of the Materials Research Society Meeting, April 2001, San Francisco, CA.

- J. G. Ryan and T. N. Theis, "Interconnects," The Encyclopedia of Materials: Science and Technology, accepted for publication.

- R. D. Goldblatt, B. Agarwala, M. B. Anand, E. P. Barth, G. A. Biery, Z. G. Chen, S. Cohen, J. B. Connolly, A. Cowley, T. Dalton, S. K. Das, C. R. Davis, A. Deutsch, C. DeWan, C. Edelstein, P. A. Emmi, C. G. Faltermeier, J. A. Fitzsimmons, J. Hedrick, J. E. Heidenreich, C. K. Hu, J. P. Hummel, P. Jones, E. Kaltalioglu, B. E. Kastenmeier, M. Krishnan, W. F. Landers, Liniger, J. Liu, N. E. Lustig, S. Malhotra, D. K. Manger, V. McGahay, R. Mih, H. A. Nye, S. Purushothaman, H. A. Rathore, S. C. Seo, T. M. Shaw, A. H. Simon, T. A. Spooner, M. Stetter, R. A. Wachnik, J. G. Ryan, "A High Performance 0.13&mu.m Copper BEOL Technology with Low-k Dielectric," Proceedings of the 2000 International Interconnect Technology Conference, June 7, 2000, Burlingame, CA.

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- A. E. Kaloyeros, S. Luryi, J. G. Ryan, and J. J. Sullivan, "High-Performance Interconnects For On-Chip Device Integration," Semiconductor International, 20 (12), pp. 115 - 122 (1997).

- J. G. Ryan, J. E. Heidenreich, W. J. Cote, R. M. Geffken and T. N. Theis, "Technology Challenges for Advanced Interconnects," invited paper in the Advanced Metallization and Interconnect Systems for ULSI Applications in 1997 Conference Proceedings, R. Cheung, J. Klein, K. Tsubouchi, M. Murakami, and N. Kobayashi editors, pp. 399 - 404, 1997.

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- J. G. Ryan, “Nanodevices,” (invited) Tutorial presented at the North Carolina Nanotechnology Commercialization Conference, 3/25/09, Raleigh, NC.

- J. G. Ryan, “Development of Government – Industry – University Consortia: Lessons Learned from IBM and CNSE,” (invited) DARPA/MTO Workshop on “Maintaining Secure IC Fabrication Capabilities for DoD and National Security Applications,” San Jose, CA, 10/9/08.

- J. G. Ryan and J. U. Lee, “Nanomaterials Innovation in Interconnect Technology,” (invited) Common Platform Technology Forum 2008, San Jose, CA, 9/30/08.

- C. Borst, S. Bennett, Z. Robinson, D. Steinke, S. McTaggart, J. G. Ryan and J.-U. Lee, “Oxide/Polysilicon CMP Process Integration for Novel Graphene and Carbon Nanotube Devices,” (invited) 13th International Conference on Chemical-Mechanical Polish Planarization for ULSI Multilevel Interconnection (CMP-MIC), Fremont, CA, 3/6/08.

- H. Meiling, V. Banine, K. Cummings, M. Goethals, N. Harned, B. Hultermans, P. Kurz, S. Lok, M. Lowisch, H. Meijer, U. Mickan, K. Ronse, J. G. Ryan, M. Tittnich and J. Zimmerman, “Field Performance of the EUV Alpha Demo Tools,” (invited), SPIE 2008, San Jose, CA, 2/26/08.

- J. G. Ryan, “Metrology Requirements for Device Scaling,” (invited) Presented as part of *Small Times* “The Impact of Imaging Advancements” Webcast, 10/30/07.

- M. Hakey, K. Rodbell, M. Van Horn and J. G. Ryan, “Supply of Advanced Microelectronics for Department of Defense and Space Applications – A Strategic Advantage for the United States,” Presented at the NanoTX Conference and Expo, Dallas, TX, 10/3/07.

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- J. G. Ryan, “Nanotechnology – Science and Current Scenario,” (invited) Presented at the Albany Law School Symposium on The Legal Future of Nanotechnology, 3/1/07, Albany, NY.

- J. G. Ryan, “Radiation Hardened Nanoelectronics Focus Center,” Presented at The Space Environmental Effects Working Group 2006 Conference, El Segundo, CA, 11/1/06.

- J. G. Ryan, D. Back, G. Denbeaux, F. Goodwin, J. Hartley, R. Housely, K. Kemp, K. Kimmel, B. LaFontaine, J. Mackey, A. Rudack, M. Tittnich, O. Wood and P. Naulleau, “EUV Lithography Programs at Albany NanoTech,” Presented at The Fourth International Symposium on EUV Lithography, San Diego, CA, 11/7/05.

- J. G. Ryan, “Industry/University/Government Partnerships for the 21st Century,” (invited) Presented at the Albany Symposium on Global Nanotechnology, Bolton Landing, NY, 9/28/05.

- J. G. Ryan and A. E. Kaloyeros, “Nanotechnology: How Will It Change Semiconductor Manufacturing,” (invited) Presented as part of the 2005 Electronics Manufacturing Summit Webcast, April 2005.

- J. G. Ryan, “Where Are We Going From Here,” (invited) Presented at Semico Impact Series: Nanotechnology Conference – Big Business in Little Things, San Jose, CA, 11/4/04.

- J. G. Ryan and A. E. Kaloyeros, “The IBM – Albany NanoTech Relationship: A New Paradigm for Industry – University Partnership,” (invited) Presented at NanoQuebec, Sherbrooke, QC, 11/14/03.

- J. C. Hedrick, C. Tyberg, E. Huang, M. Sankarapandian, K. Malone, S. T. Chen, S. Nitta, C. Narayan, S. Purushothaman, and J. Ryan, "Low-k Dielectric Materials for High Performance Interconnects," Presented at the American Chemical Society National Meeting, 4/10/02.

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- J. G. Ryan, M. B. Anand, G. A. Biery, C. R. Davis, T. Dalton, R. Dellaguardia, P. Duncombe, D. C. Edelstein, S. Gates, S. Greco, J. Hedrick, P. Jones, M. Lane, V. McGahay, C. Narayan, S. Nitta, S. Purushothaman, T. M. Shaw, T. A. Spooner, and R. D. Goldblatt, "Copper and Low-k Dielectric Integration Challenges," (invited) Proceedings of SEMICON West 2000 Technical Sessions, 7/10/00, San Francisco, CA.

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- J. G. Ryan, R. Goldblatt, V. McGahay, C. Davis, C. Narayan, J. Hedrick, J. Hay, D. Edelstein, S. T. Chen, and K. Rodbell, "Directions and Challenges in Low-k Integration," (invited) Presented at the Clarkson University 4th International CMP Symposium, Lake Placid, NY, 8/9/99 - 8/11/99.

- J. G. Ryan, S. Purushothaman, J. Harper, J. Hedrick, K. Rodbell, D. Edelstein, J. Hay, J. Hummel, and T. Theis, "Technology Challenges for Advanced Interconnects," (invited) Presented at the 1st International Conference on Advanced Materials and Processes for Microelectronics, March 15 - 18, 1999, San Jose, CA and as a seminar in the MIT Microsystems Technology Laboratories VLSI Seminar Series, March 16, 1999.

- J. G. Ryan, "Cu Interconnect Technology Challenges - Rump Session Presentation," 1998 VLSI Symposium, 6/9/98 - 6/11/98, Honolulu, Hawaii.

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- J. G. Ryan, "Technology Challenges for Advanced Interconnect Structures in Integrated Circuits," Seminars presented to the Materials Science Department of The University of Michigan, 3/20/98 and at the CAIST Seminar Series at Rensselaer Polytechnic Institute, 3/24/98.

- G. S. Akiki and J. G. Ryan, "Key Technology Challenges for Advanced Semiconductor Processing," Clarkson University CAMP Meeting, 11/6/97, Potsdam, NY.

- G. Ouimet, F. Schmidt, A. Ticknor, K. Boggs, K. Davis, W. Landers and J. G. Ryan, "Key Technology Challenges for CMP," Clarkson University CAMP Annual Technical Meeting, 5/21-23/97, Lake Placid, NY. (invited)

- J. G. Ryan, T. E. Sandwick, and W. F. Landers, "Chemical Mechanical Polishing: Applications and Challenges," Clarkson University CAMP Annual Technical Meeting, 5/15-17/96, Lake Placid, NY. (invited)

- J. G. Ryan, "Interconnection Technology Trends," CAT Seminar Series, University at Albany, SUNY, 11/13/95.

- J. G. Ryan, "Applications Of Collimated Sputtering," CAT Seminar Series, University at Albany, SUNY, 11/21/95.

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- T. Licata, D. Strippe, T. McDevitt, Jerome B. Lasky and J.G. Ryan, "Collimated Sputtering for Enhanced Fill and Evaluation of Film Properties," Presented at the 39th National AVS Symposium and Topical Conferences, Seattle, 1992.

- J.B. Riendeau, T.D. Sullivan, and J.G. Ryan, "Characterization of Thermally Induced Voiding in AlSi Interconnects," Presented at 38th Annual AVS Symposium and Topical Conference, Seattle, 1992.

- D. Strippe, T. Licata, R. Bass, and J.G. Ryan, "The Effect of Arrival Angle on the Microstructure of Reactively Sputtered Titanium Nitride," Presented at the 1991International Conference on Metallurgical Coatings and Thin Films, San Diego, CA.

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- S. Roberts, J.G. Ryan, M.H. Ishaq, and J. Baglin, "Studies of Evaporated Silicon- Rich Silicides," Electrochemical Society Extended Abstract 223,360 (1982).

- A. Zelman, J.G. Ryan, D. Smith, and D. Gisser, "Electroosmotic Processing of Cryo-Preserved Red Blood Cells," Presented at 1980 FASEB Meeting.

Panels, Rump Sessions, Course Organizer

- Panelist, "Super Trend Convergence: How Leaders Will Deal with the Great Changes Ahead," Leadership Greensboro Forum, Greensboro, NC, 9/25/09.

- Panelist, "Roundtable – Key Issues and Next Steps Forward," National Academy of Science Meeting on The Future of Photovoltaic Manufacturing in the United States, Washington, DC, 4/23/09.

- Panelist, Semiconductor International's technology webcast panel on "Nanotech's Role in Post-CMOS Production," January 16, 2007.

- Panelist, Semiconductor International's technology webcast panel on "Advanced Material Solutions for Interconnects," 9/13/06.

- Panelist, Applied Materials sponsored panel on "The Patterning Challenge: What makes sense for 45 nm and beyond?" at IITC, Burlingame, CA, 6/5/06.

- Chair, Nanoelectronics Panel, The First Annual Axiom Capital Management – Livingston Nanotechnology Conference, New York, NY 12/7/05.

- Panelist, Chartered Technology Forum, San Jose, CA 9/22/05.

- Panelist, Summit in Tech Valley, Colonie, NY 4/26/05.

- Course Organizer for "Advanced Interconnects: Design, Process and Integration," 2000 IEDM Short Course.

- Co-Chair for VLSI Symposium's Rump Session on Advanced Metallization (1998)

Non-Technical Presentations (unpublished)

- J. G. Ryan, "The Joint School of Nanoscience and Nanoengineering," (invited) Presented at Greensboro Rotary Club Luncheon," Greensboro, NC, 9/16/09, Greensboro Airport Rotary Club Breakfast, Greensboro, NC 10/20/09 and Guilford County Rotary Club Luncheon, Greensboro, NC 12/1/09.

- J. G. Ryan, "The Joint School of Nanoscience and Nanoengineering," (invited) Presented at Action Greensboro's forum "Higher Education as an Economic Engine," Greensboro, NC, 9/10/09.

- J. G. Ryan, "The Joint School of Nanoscience and Nanoengineering," (invited) Presented to the North Carolina Senate Select Committee on Energy, Science and Technology, Raleigh, NC, 4/29/09.

- J. G. Ryan, "Innovation Collaboration: Academic, Corporate and Governmental Roles in Research and Entrepreneurship" (invited) Presentation at Brooks Pierce Law Firm Event "The Upside of a Downturn: Opportunities for Entrepreneurs", 1/22/09.

- J. G. Ryan, "Intro to Nanotechnology," (invited) Presentation at Hudson Valley Community College's Career Exploration Day, Troy, NY, 11/1/07.

- J. G. Ryan, "CNSE-University Partnerships: A New Paradigm for R & D in the 21st Century," (invited) 2006 IEEE International SOI Conference, Niagra Falls, NY, 10/3/06.

- J. G. Ryan, "Programs and Partnerships for the High Tech Economy of the 21st Century," (invited) Presented at CIREB, Latham, NY, 12/1/05.

- J. G. Ryan, "IBM Microelectronics Interactions with the University at Albany," University at Albany Industry Day Conference, Albany, NY, 4/20/99.

- J. G. Ryan, "Tips for Job Seeking Technical Professionals," Employment Seminar, American Vacuum Society 43rd National Symposium, Philadelphia, PA, 10/15/96.

- J. G. Ryan, "IBM & Center for Advanced Thin Film Technology Partnering," Industry Day Conference, New York State Center for Advanced Thin Film Technology, University at Albany, State University of New York, 10/2/96

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- J.E. Cronin and J.G. Ryan, "Micromachine Transfer Belt Data Tape Process," IBM TDB, 34 (7B), 147, 1991. (Published anonymously)

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- L.A. Nesbit, P. Pan, and J.G, Ryan, "Low Resistivity Stack for Dual Doped Polysilicon Gate Electrode," Research Disclosure, 326, 32630, 1991. (Published anonymously)

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